SPECIFICATION OF THE DIGITAL AUDIO INTERFACE
(The AES/EBU interface)

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CONTENTS

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Specification of the digital audio interface (The AES/EBU interface)

1. Scope

This document specifies a recommended interface for the serial digital transmission of two channels of periodically sampled and linearly represented digital audio data in a broadcasting complex, up to a distance of a few hundred metres,

Although this transmission specification is independent of sampling frequency the interface is primarily intended to be used at 48 kHz as this is the recommended sampling frequency for use in broadcasting studios (CCIR Recommendation 646).

The document does not cover connection to any common carrier equipment nor does it specifically address any of the questions relating to the synchronising of large systems, although by its nature the format permits easy synchronisation of receiving devices to the transmitting device.

Specific synchronisation issues are covered in document AES 1l-l991.

Note 1: In this interface specification for broadcasting studio use, mention is also made of an interface for consumer use. The two interfaces are not identical.

Note 2: An engineering guideline document to accompany this interface specification is in course of preparation by the EBU.

2. Interface format

2.1. Terminology

For the purpose of this specification the following definitions of terms apply.

2.1.1. Sampling Frequency

The sampling frequency is the frequency of the samples representing an audio signal. When more than one audio signal is transmitted through the same interface, the sampling frequencies shall be identical.

2.1.2. Audio sample word

The audio sample word represents the amplitude of a digital audio sample. Representation is linear in 2's complement binary form. Positive numbers correspond to positive analogue voltages at the input of the analogue to digital convertor (ADC). The number of bits per word can be specified from 16 to 24 in two coding ranges (less than or equal to 20 bits and less than or equal to 24 bits).

2.1.3. Auxiliary sample bits

The four least significant bits (LSB) can be assigned as auxiliary sample bits and used for auxiliary information when the number of audio sample bits is less than or equal to 20.

2.1.4. Validity bit

This bit indicates whether the audio sample bits in the sub-frame (time slots 4-27 or 8-27 depending on the audio word length as described in *Section 2.2.1.*) are suitable for conversion to an analogue audio signal.

2.1.5. Channel status

The channel status carries, in a fixed format derived from the block (see *Section 2. 1. 11.*), information associated with each audio channel which is decodable by any interface user.

2.1.6. User data

The user data channel is provided to carry any other in formation.

2.1.7. Parity bit

The parity bit is provided to permit the detection of an odd number of errors resulting from malfunctions in the interface.

2.1.8. Preambles

Preambles are specific patterns used for synchronisation. There are three different preambles (see Section 2.4.).

2.1.9. Sub-frame

The sub-frame is a fixed structure used to carry the information described in *Sections 2.1.1.* to *2.1.8.* (see *Sections 2.2.1.* and *2.2.2.*).

2.1.10. Frame

The frame is a sequence of two successive and associated sub-frames.

2.1.11. Block

The block is a group of 192 consecutive frames. The start of a block is designated by a special sub-frame preamble (see *Section 2.4.*).

2.1.12. Channel coding

The channel coding describes the method by which the binary digits are represented for transmission through the interface.

2.2. Structure of format

2.2.1. Sub-frame format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31 (see fig 1)

Time slots 0 to 3 (preamble) carry one of the three permitted preambles (see *Fig.* 2) (see *Sections* 2.2.2. and 2.4.; see also *Fig.* 2).

Tune slots 4 to 27 *(audio samples word)* carry the audio sample word in linear 2's complement representation. The most Significant bit (MSB) is carried by time slot 27.

When a 24-bit coding range is used, the LSB is in time slot 4 (see *Fig. 1a).*

When a 20-bit coding range is sufficient, time slots 8-27 carry the audio sample word with the LSB in time slot 8. Time slots 4 to 7 may be used for other applications. Under these circumstances, the bits in the time slots 4 to 7 are designated auxiliary sample bits. (see Fig. 1b)

If the source provides fewer bits than the interface allows (either 24 or 20) the unused LSB shall be set to logic “0”.

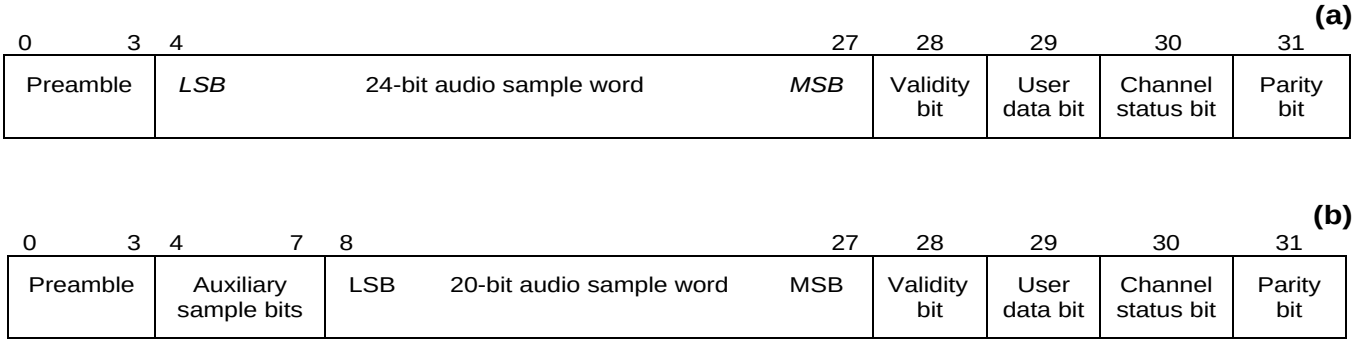


Fig. 1 – Sub-frame format for audio sample words of 24 bits (top) and 20 bits (bottom).

Time slot 28 (validity bit) carries the validity bit associated with the audio sample word (see *Section 2.5).*

Time slot 29 (user data bit) carries one bit of the user data channel associated with the audio channel transmitted in the same sub-frame (see *Section 3).*

Time slot 30 (channel status bit) carries one bit of the channel status information associated with the audio channel transmitted in the same sub-frame (see *Section 4).*

Time slot 31 (parity bit) carries a parity bit such that time slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros (even parity).

Note: The preambles have even parity as an explicit property.

2.2.2. Frame format

A frame is uniquely composed of two sub-frames *(see Fig.* 2). The rate of transmission of frames corresponds exactly to the source sampling frequency.

The first sub-frame normally starts with preamble "X", however the preamble changes to preamble "Z" once every 192 frames. This defines the block structure used to organise the channel status information. The second sub-frame always starts with preamble “Y”.

The modes of transmission are signalled by setting bits 0 to 3 of byte 1 of channel status.

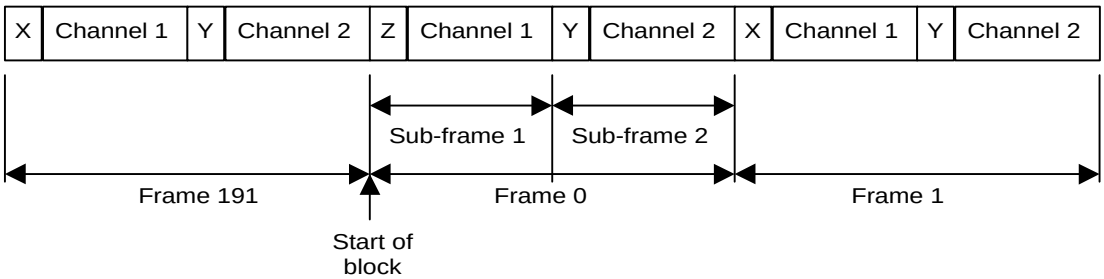


Fig. 2 - Frame format

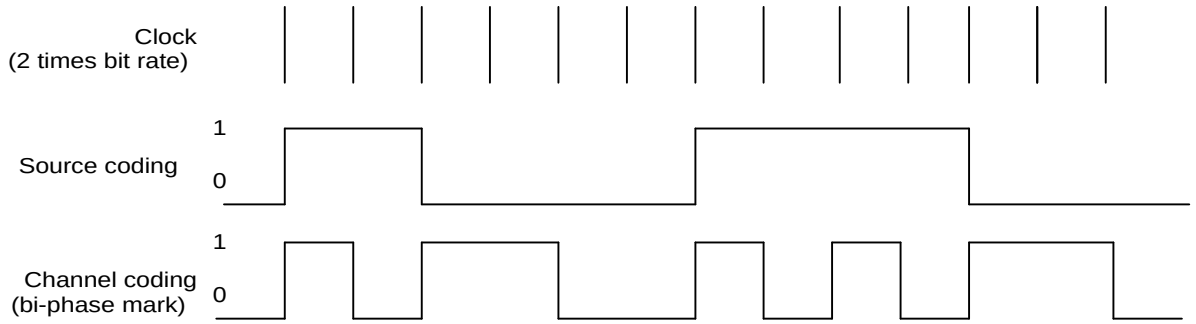


Fig. 3 - Channel coding

a) 2-channel mode

In 2-channel mode the samples from both channels are transmitted in consecutive sub-frames. Channel 1 is in sub-frame 1 and channel 2 is in sub-frame 2.

b) Stereophonic mode

In stereophonic mode the interface is used to transmit stereophonic audio in which the two channels are presumed to have been simultaneously sampled. The left or "A" channel is in sub-frame 1 and the right or "B" channel is in sub-frame 2.

c) Single channel mode (monophonic)

In monophonic mode the transmitted bit rate shall remain at the normal 2-channel rate and the audio sample word shall be placed in sub-frame 1. Time slots 4 to 31 of sub-frame 2 shall either carry the identical bits to sub-frame 1 or shall be set to logic "0'. A receiver shall normally default to channel 1 unless manual override is provided.

(d) Primary/Secondary mode

In some applications requiring two channels where one of the channels is the main or primary channel while the other is a secondary channel, the primary channel is in sub-frame 1 and the secondary channel is in sub-frame 2,

2.3. Channel coding

To minimise the direct current (DC) component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in bi-phase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logic "0", however, it is different if the bit is logic "1" (see *Fig. 3).*

2.4. Preambles

Preambles are specific patterns providing synchronisation and identification of the sub-frames and blocks.

To achieve synchronisation within one sampling period and to make this process completely reliable, these patterns violate the biphase mark code rules. Thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots at the start of each sub-frame (time slots 0 to 3) and are represented by eight successive states.

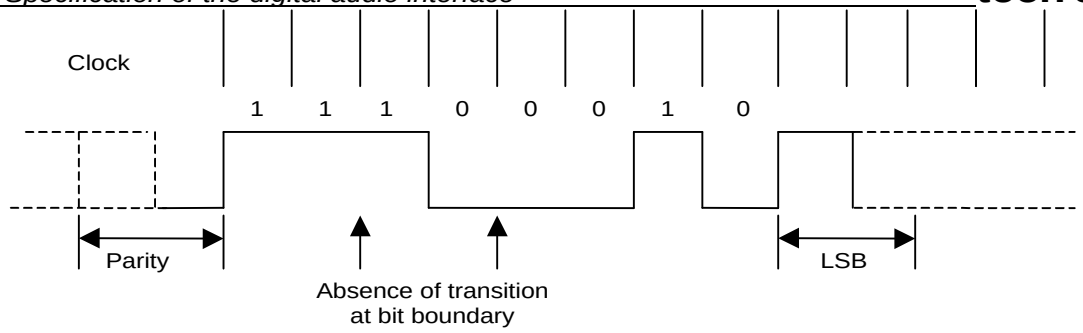


Fig. 4 Preamble "X" (11100010)

The first stale of the preamble is always different from the second state of the previous symbol (representing the parity bit). Depending on this state the preambles are:

Preceding state:	0	1	
	channel coding		
"X"	11100010	00011101	Sub-frame 1
"Y"	11100100	00011011	Sub-frame 2
"Z"	11101000	00010111	Sub-frame 1 + block start

Like biphase code, these preambles are DC free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

Fig. 4 represents preamble "X".

Note: Owing to the even parity bit in time slot 31, all preambles will start with a transition in the same direction (see *Section 3.2.*1.). Thus only one of these sets of preambles will, in practice, be transmitted through the interface. However, it is necessary for either set to be decodable because a polarity reversal may occur in the connection.

2.5. Validity bit

The validity bit shall be logic "0" if the audio sample word is suitable for conversion to an analogue audio signal and it shall be logic "1" if it is not.

There is no default state for the validity bit

3. User data format

User data bits may be used in any way desired by the user.

Possible formats for the user data channel are indicated by channel status byte 1 bits 4-7.

The default value of the user data bit shall be logic "0".

4. Channel status format

The channel status for each audio signal carries information associated with that audio signal, and thus it is possible for different channel status data to be carried in the two sub-frames of the digital audio signal. Examples of information to be carried in the channel status are: length of audio sample words; number of audio channels, sampling frequency, time code, alphanumeric source and destination codes, and pre-emphasis.

Channel status information is organised in 92-bit blocks, subdivided into 24 bytes (Fig. 5). The first bit of each block is carried in the Frame with preamble "Z".

The specific organisation follows, wherein the suffix 0 designates the first byte or bit.

	Bit							
Byte	0	1	2	3	4	5	6	7
0	Use of channel status channel	Audio/non-audio use	Audio signal emphasis			Locking of source sample frequency	Sampling frequency	
1	Channel mode				User bit management			
2	Use of auxiliary sample bits			Source word length & source encoding history			Reserved	
3	Future multichannel function description							
4	Digital audio reference		Reserved					
5	Reserved							
6	Alphanumeric channel origin data							
7								
8								
9								
10	Alphanumeric channel destination data							
11								
12								
13								
14	Local sample address code (32-bit binary)							
15								
16								
17								
18	Time-of-day sample address code (32-bit binary)							
19								
20								
21								
22	Reliability flags							
23	Cyclic redundancy check character							

Fig. 5 - Channel status data format

Byte 0

Bit 0

0 Consumer use of channel status block (see *Note)*
1 Professional use of channel status block

Bit 1

0 Normal audio mode
1 Non-audio mode

Bits 2 to 4 Encoded audio signal emphasis

Bit state			
0	0	0	Emphasis not indicated. Receiver defaults to no emphasis with manual over-ride enabled.
1	0	0	No emphasis. Receiver manual over-ride disabled.
1	1	0	50/15 µs emphasis. Receiver manual over-ride disabled.
1	1	1	CCITT J.1 7 emphasis (with 6.5dB insertion loss at 500Hz). Receiver manual over-ride disabled.

All other slates of bits 2-4 are reserved and are not to be used until further defined.

Bit 5

0 Default, and source sampling frequency locked.
1 Source sampling frequency unlocked.

Bits 6-7 Encoded sampling frequency

Bit state	6	7	
	0	0	Sampling frequency not indicated. Receiver default to 48 kHz: manual over-ride or auto set enabled.
	0	1	48 kHz sampling frequency. Manual over-ride or auto set disabled.
	1	0	44.1 kHz sampling frequency. Manual over-ride or auto set disabled.
	1	1	32 kHz sampling frequency. Manual over-ride or auto set disabled.

Note: The significance of byte 0 Bit 0 is such that a transmission from an interface conforming to IEC 958 "consumer use" can be identified, and receiver conforming only to IEC 958 "consumer use" will correctly identify a transmission from a "professional use" interface as defined in this standard. Connection of a "professional use" transmitter with a "consumer use receiver or vice versa might result in unpredictable operation.

Byte 1

Bits 0-3 Encoded channel mode

Bit state	0	1	2	3	
	0	0	0	0	Mode not indicated. Receiver default to two-channel mode. Manual over-ride enabled.
	0	0	0	1	Two-channel mode. Manual over-ride disabled.
	0	0	I	0	Single-channel mode (monophonic). Manual over-rIde disabled.
	o	0	1	1	Primary! secondary mode (sub-frame I is primary). Manual over-ride disabled.
	0	1	0	0	Stereophonic mode (channel 1 is left channel). Manual over-ride disabled.
	0	1	0	1	Reserved for user-defined applications.
	0	I	1	0	Reserved for user-defined applications.
	1	1	1	1	Vector to byte 3. Reserved for future applications.

All other states of bits 0-3 are reserved and are not to be used until further defined.

Bits 4-7 Encoded user bits management

Bit state	4	5	6	7	
	0	0	0	0	Default. No user information indicated.
	0	0	0	1	1 92~bit block structure. Preamble "Z" indicates the start of a block.
	0	0	1	0	Packet system based on HDLC protocol (see Note).
	0	0	1	1	User defined.

All other states of bits 4-7 are reserved and are not to be used until further defined.

Note: This system is defined in Supplement 1 to EBU Tech. 3250: format of the user data channel of the digital audio interface.

Byte 2					
Bits 0-2				Encoded use of auxiliary sample bits	
Bit	0	1	2		
state	0	0	0	Maximum audio sample word length is 20 bits (default). Use of auxiliary sample bits not defined,	
	0	0	1	Maximum audio sample word length is 24 bits, Auxiliary sample bits used for main audio sample data	
	0	1	0	Maximum audio sample word length is 20 bits, Aux. sample bits carry a single coordination signal (Note 1)	
	0	1	1	Reserved for user-defined applications	
	All other states of bits 0-2 are reserved and shall not be used until further defined				
Bits 3-5				Encoded audio sample word length of transmitted signal (Notes 2, 3 and 4)	
Bit	3	4	*5*	*Audio sample word length H maximum length is 24 bits, as indicated by bits 0-2 above*	*Audio sample word length if maximum length is 20 bits, as indicated by bits 0-2 above*
state	0	0	0	Word length not indicated (default)	Word length not indicated (default)
	0	0	1	23 bits	19 bits
	0	1	0	22 bits	18 bits
	0	1	1	21 bits	17 bits
	1	0	0	20 bits	16 bits
	1	0	1	24 bits	20 bits
	All other states of bits 3 - 5 are reserved and shall not be used until further defined,				
Bits 6-7	Reserved, and shall be set to logic "0 until further defined.				

Note 1: The signal coding used for the co-ordination channel is described in *Appendix 1* to this document.

Note 2 The default state of bits 3-5 indicates that the number of active bits within the 20 or 24 bits coding range is not specified by the transmitter. The receiver should default to the maximum number of bits specified by the coding range and enable manual override or auto set.

Note 3 The non-default states of bits 3-5 indicate the number of active bits within the 20 or 24 bits coding range which might be active. This is also an indirect expression of the number of LSBs that are certain to be inactive which is equal to 20 or 24 minus the number corresponding to the bit state, The receiver should disable manual override and auto set for these bit states,

Note 4: Irrespective of the audio sample word length as indicated by any of the states of bits 3-5, the MSB is in time slot 27 of the transmitted sub-frame as specified in *Section 2.2.1,*

Byte 3	
Bits 0-7	Vectored target byte from byte 1 Reserved for future use as multi-channel function description. Shall be set to logic "0"at present

Byte 4				
Bits 0-1			Digital audio reference signal (as per AES11-1991)	
Bit	0	1		
state	0	0	Not a reference signal (default).	
	0	1	Grade 1 reference signal.	
	1	0	Grade 2 reference signal.	
	1	1	Reserved and shall not be used until further defined.	
Bits 2-7	Reserved, and shall be set to logic "0" until further defined.			

Byte 6-9 Alphanumeric channel origin data. First character in message is byte 6.	
Bits 0-7 (each byte)	7-bit ISO 646 (ASCII) data with no parity bit. LSBs are transmitted first with logic "0" in bit 7. Non-printed control characters (codes 01 hex to 1F hex and 7Fhex) are not permitted. Default value shall be logic "0" (code 00hex ASCII "NULL")

Byte 10-13 Alphanumeric channel destination data. First character in message is byte 10.	
Bits 0-7 (each byte)	7-bit ISO 646 (ASCII) data with no parity bit. LSBs are transmitted first with logic "0" in bit 7. Non-printed control characters (codes 01 hex to 1F hex and 7Fhex) are not permitted. Default value shall be logic "0" (code 00_{hex} ASCII "NULL")

Byte 14-17 Local sample address code (32-bit binary). Value is first sample of current block.	
Bits 0-7 (each byte)	LSBs are transmitted first. Default value shall be logic "0".

Note: This has the same function as a recording index counter.

Byte 18-21 Time of day sample address code (32-bit binary). Value is first sample of current block.	
Bits 0-7 (each byte)	LSBs are transmitted firs!. Default value shall be logic "0".

Note: This is the time-of-day laid down during the source encoding of the signal and shall remain unchanged during subsequent operations. A value of all zeros for the binary sample address code shall, for the purposes of transcoding to real time, or to time codes in particular, be taken as midnight (i.e. 00 h, 00 mm, 00 s, 00 frame). Transcoding of the binary number to any conventional time code requires accurate sampling frequency information to provide the sample accurate time.

Byte 22 Flag used to identify whether the information carried by the channel status data is reliable. According to the following table, if reliable the appropriate bits shall be set to logic "0" (default). if unreliable the bits shall be set to logic '1".	
Bits 0-3	Reserved. and shall be set to logic "0" until further defined.
Bit 4	Bytes 0 to 5
Bit 5	Bytes 6 to 13
Bit 6	Bytes 14 to 17
Bit 7	Bytes 18 to 21

Byte 23 Channel status data cyclic redundancy check character (CRCC).	
Bits 0-7	Generating polynomial is; $G(X) = X^8 + X^4 + X^3 + X^2 + 1$ The CRCC conveys information to test valid reception of the entire channel status data block (bytes 0 to 22 inclusive). For serial implementations, the initial condition of all logic "1"s should be used when generating the check bits, with the LSB transmitted first. Default value shall be logic "0" for minimum implementation of channel status only (see *Section 5.2.1.).*

Note: *Appendix2* includes a diagram of the shift register circuit used togenerate the code and two examples of channel status data, and the corresponding CRC byte.

5. Interface format implementation

5.1. General

To promote compatible operation between items of equipment built to this specification it is necessary to establish which information bits and operational bits need to be encoded and sent by a transmitter and decoded by an interface receiver.

Documentation shall be provided describing the channel status features supported by the interface transmitters and receivers.

5.2. Transmitter

Transmitters shall follow all the formatting and channel coding rules established in earlier sections of this specification. Along with the audio sample word, all transmitters shall correctly encode and transmit the validity hit, user bit, parity bit, and the three preambles. The channel status shall be encoded to one of the implementations given below.

The following three implementations are defined: "minimum", "standard", and "enhanced". These terms are used to communicate in a simple manner the level of implementation of the interface transmission involving the many features of channel status. Irrespective of the level of implementation the reserved states of bits defined in section 4 shall remain unchanged.

5.2.1. Minimum implementation of channel status

The *minimum* implementation represents the lowest level of implementation of' the interface that meets the requirements of this specification document. In the minimum implementation, transmitters shall encode and transmit channel status byte 0, bit 0 with a state of logic "1" signifying "professional use of channel status block". All other channel status bits of Bytes 0 to Byte 23 inclusive shall be transmitted with the default state of logic "0". In this circumstance, the receiver will adopt the default conditions specified in bytes 0 to 2.

If additional bytes of channel status (which do not fully comply with the standard implementation see Section 5.2.2.) are implemented as required by an application the interface transmitter shall be classified as a minimum implementation of channel status.

It should be noted that this implementation imposes severe operational restrictions on the receiving devices which may be connected to it. For example, receivers implementing byte 23 will show a CRC error when the default value of logic "0" is received as the CRCC. Also, reception of the default value for byte 0 bits 6-7 might cause improper operation in receiving devices not supporting manual override or auto set capabilities.

5.2.2. Standard implementation of channel status

The standard implementation provides a fundamental level of implementation which should prove sufficient for general applications in professional audio or broadcasting. In addition to conforming to the requirements described above for the minimum implementation, a standard implementation interface transmitter shall correctly encode and transmit all channel status bits in byte 0, byte 1, byte 2 and byte 23 (CRCC) in the manner specified in this document.

5.2.3. Enhanced implementation of channel status

In addition to conforming to the requirements described above for the standard implementation, the *enhanced* implementation shall provide further capabilities.

5.3. Receivers

Implementation in receivers is highly dependent on the application. Proper documentation shall be provided on the level of implementation of the interface receiver for decoding the transmitted information (validity. user, channel status, parity), and on whatever subsequent action is taken by the equipment of which it is a part.

6. Electrical requirements

6.1. General characteristic

The electrical parameters of the interface are based on those defined in CCITT Recommendation V.11 for balanced voltage digital circuits which allow signal transmission over distances of up to a few hundred meters.

In order to improve the balance of the transmitter or the receiver or both beyond that recommended by the CCITT, a circuit conforming to the general configuration shown in *Fig. 6* shall be used.

In this circuit the series capacitors C2 and C3 isolate the transformers and prevent damage from connection to a source containing a DC voltage. In addition to achieving higher rejection of common mode signals, the transformers reduce grounding and electromagnetic interference (EMI) problems. Although equalization may be employed at the receiver, no equalization prior to transmission is permitted.

The interconnecting cable shall be balanced and screened (shielded) with nominal characteristic impedance of 110 Ω at frequencies from 0.1 to 6.0 MHz.

6.2. Line driver characteristics

6.2.1. Output impedance

The line driver shall have a balanced output with an internal impedance of 110 Ω ± 20%, at frequencies from 0.1 to 6.0 MHz when measured the output at terminals.

6.2.2. Signal amplitude

The signal amplitude shall lie between 2 and 7 V peak-to-peak, when measured across a 110 Ω resistor connected to the output terminals, without any interconnecting cable present.

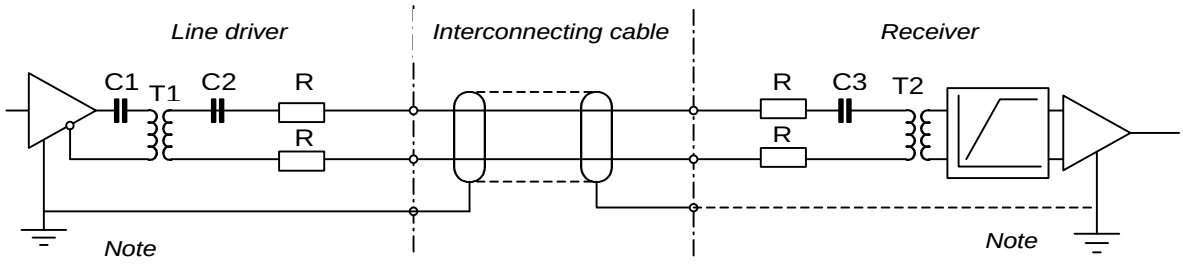


Fig. 6 - General circuit configuration.

Note Signal ground may be further connected to external protective ground if national regulations require.

6.2.3. Balance

Any common mode component at the output of the equipment shall be more than 30 dB below the signal at frequencies from DC to 6 MHz.

6.2.4. Rise and fall times

The rise and fall times determined between the 10% and 90% amplitude points, shall be between 5 ns and 30 ns when measured across a 110 Ω resistor connected to the output terminals, without any interconnecting cable present.

Note: Operation toward the lower limit of 5 ns will improve the received eye pattern but will increase EMI at the transmitter. Equipment must meet local regulations regarding EMI.

6.2.5. Data jitter

Data transitions shall occur within ±20 ns of an ideal jitter free clock measured at the half-voltage points.

Note: This specification applies only to the signal after channel coding. Tighter 5pecifleations apply to the audio sample clock.

6.3. Line receiver characteristics

6.3.1. Terminating impedance

The receiver shall present a substantially resistive impedance of 110 ± 20% to the interconnecting cable over the frequency hand 0.1 to 6.0 MHz, when measured across the input terminals. The application of more than one receiver to any one line might create transmission errors due to the resulting impedance mis-match.

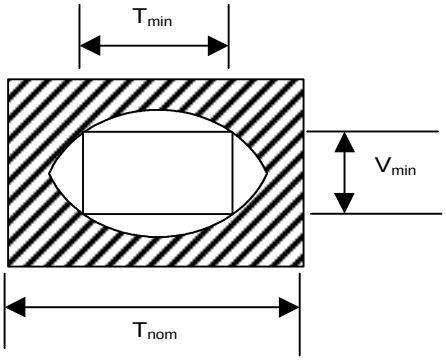
6.3.2. Maximum input signals

The receiver shall correctly interpret the data when connected directly to a line driver working between the extreme voltage limits specified by Section 6.2.2.

Note: In EBU document Tech. 3250 (1985) the specification for line driver signal amplitude was 10 V peak-to- peak maximum.

6.3.3. Minimum input signals

The receiver shall correctly sense the data when a random input signal produces the eye diagram characterised by a V_{min} of 200 mV and T_{min} of 50% of T_{nom} (see Fig. 7).



T_{min} = 0.5 x T_{nom}
V_{min} = 200 mV
T_{nom} = one-half of biphase symbol period

Fig. 7 - Eye diagram

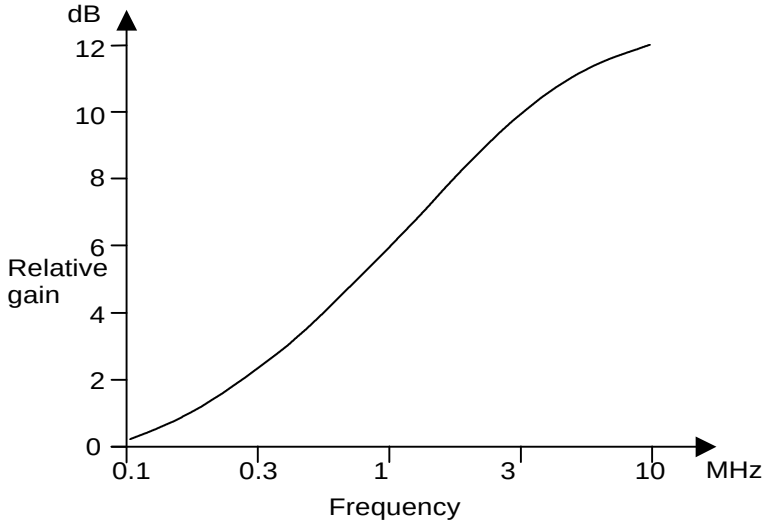


Fig. 8 - suggested equalizing characteristic for the receiver.

6.3.4. Receiver equalization

Optional equalization can be applied in the receiver to enable interconnecting cable longer than 100 m to be used. A suggested frequency equalizing characteristic is shown in Fig. 8. The receiver shall meet the requirements specified in Sections 6.3.2. and 6.3.3.

6.3.5. Common mode rejection

There shall be no data errors introduced by the presence of a common mode signal of up to 7 V peak at frequencies from DC to 20 kHz.

6.4. Connectors

The standard connector for both outputs and inputs shall be the circular latching three-pin connector described in IEC 268-12 (this type of connector is normally called "XLR").

An output connector fixed on an item of equipment shall use male pins with a female shell. The corresponding cable connector shall thus have female pins with a male shell.

An input connector fixed on an item of equipment shall use female pins with a male shell and the corresponding cable connector shall thus have male pins with a female shell, The pin usage shall be:

- pin 1: cable shield or signal earth,
- pin 2: signal
- pin 3: signal

(Note that the relative polarity of pins 2 and 3 is not important in the digital case).

Equipment manufacturers should clearly label digital audio inputs and outputs as such, including the terms "digital audio input" or "digital audio output" as appropriate.

In such cases where panel space is limited and the function of the connector might be confused with an analogue signal connector, the abbreviations "DI" and "DO" should be used to designate digital audio inputs and outputs, respectively.

Appendix 1
The provision of additional, voice-quality channels via the digital audio interface

When a 20-bit coding range is sufficient for the audio signal, the four auxiliary sample bits can be used for a voice-quality co-ordination signal (talk-back).

The voice-quality signal is sampled at exactly one-third of the sampling frequency for the main audio, coded uniformly with 12 bits/sample represented in 2's complement form. It is sent four bits at a time in the auxiliary sample bits of the interface sub-frames. One such signal may be sent in sub-frame 1 and another in sub-frame 2. The "Z" preamble at the start of each block is used as a frame alignment word for the voice-quality signals. The two sub-frames of frame 0 each contain the four LSBs of a sample of their respective voice quality signal, as shown in Fig. A. 1. This figure also shows two voice-quality signals, one in each sub-frame.

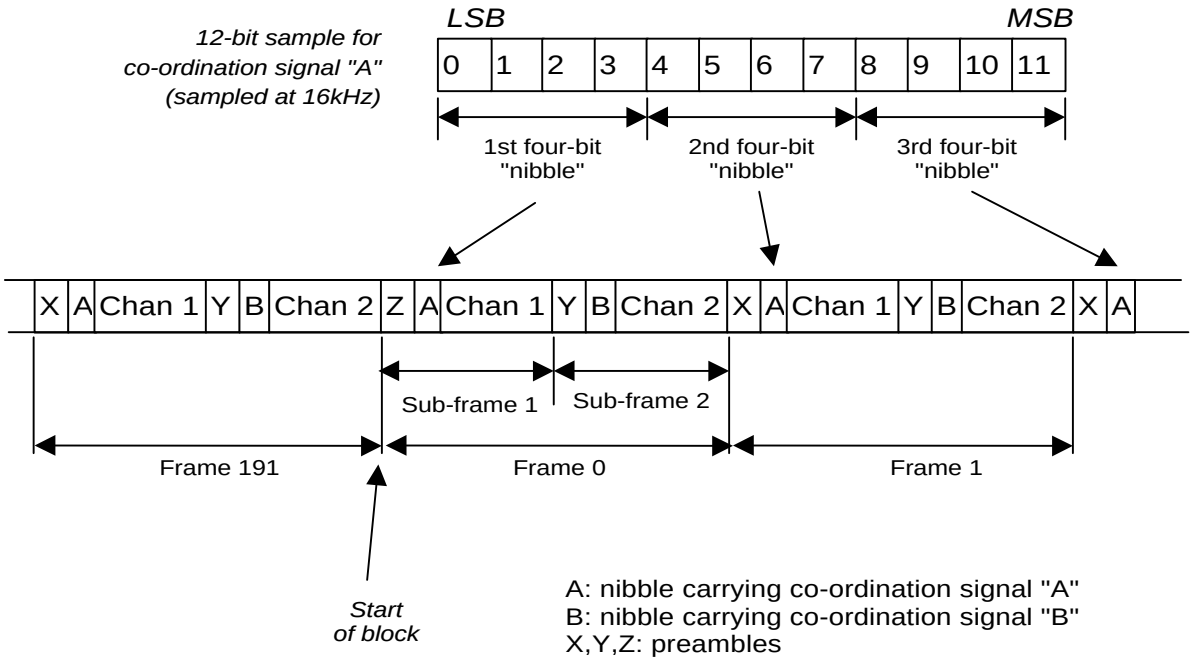


Fig. A.1. - Frame and block structure for voice-quality channels

Appendix 2
Generation of the CRCC (byte 23) for channel status

The channel status clock format of 192 bits includes a cyclic redundancy check (CRC) code which occupies the last 8 bits of the block (byte 23). The specification for the code is given by the generating polynomial:

$$G(X) = x^8 + x^4 + x^3 + x^2 + 1$$

An example of a hardware realisation in the serial form is given in *Fig. A.2.* The initial condition of all the stages is logic "1".

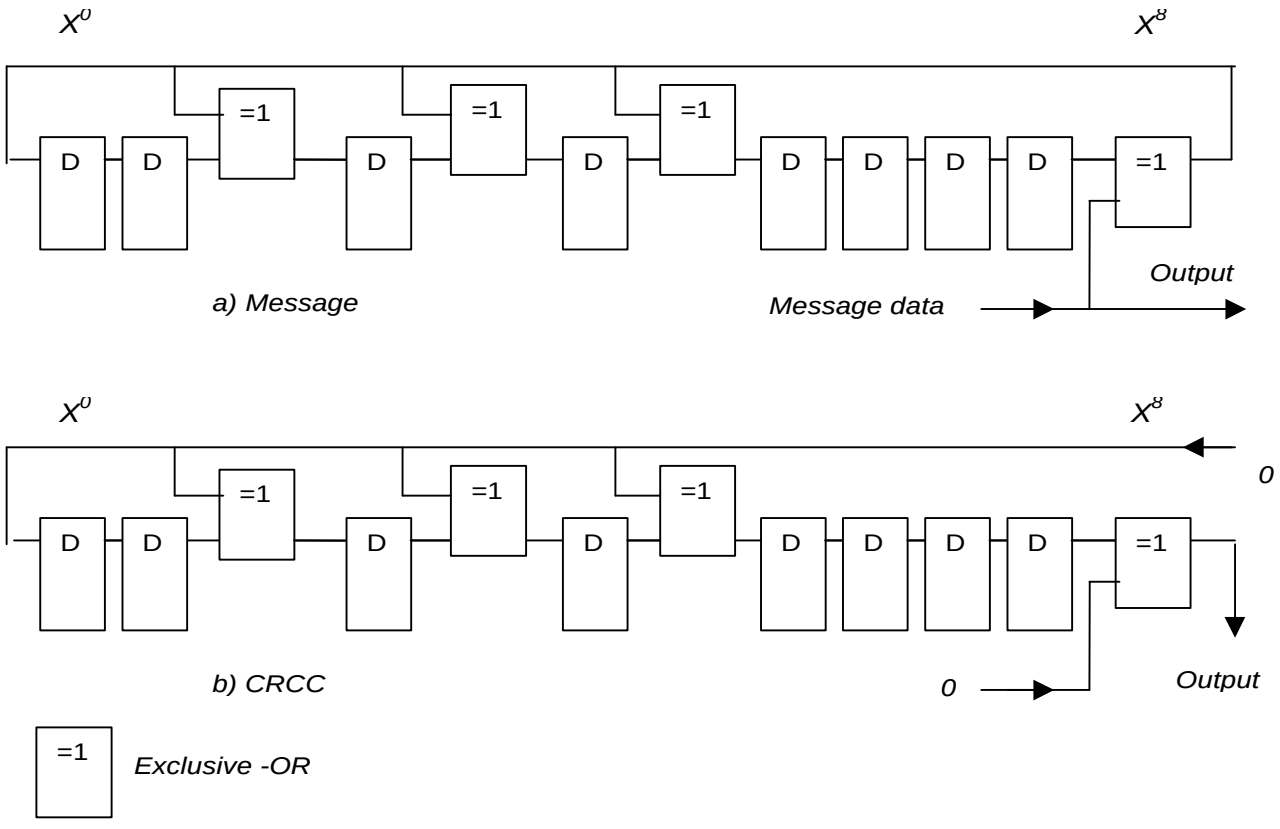


Fig. A.2. - Flow diagram of an example realisation of the CRCC generator.

Two examples of the channel status data and the resultant CRCC follow:

Example 1

Content of channel status data (bytes 0 to 022 inclusive):

Byte	Bits set to logic "1"
0	0,2,3,4,5
1	1
4	1

All other bits in channel status bytes 0 to 22 inclusive set at logic "0".

Content of CRCC (byte 23):

	1	1	0	1	1	0	0	1
Channel status bit:	184							191

Example 2

Content of channel status data (bytes 0 to 22 inclusive):

Byte	Bits set to logic "1"
0	0

All other bits in channel status bytes 0 to 22 inclusive set at logic "0".

Content of CRCC (byte 23):

	0	1	0	0	1	1	0	0
Channel status bit:	184							191

Note: No particular level of implementation should be taken as implied by the examples given in this *Appendix.*

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